

Application No. 10/068,534
Reply to Office Action dated April 5, 2005

REMARKS

Claims 1-9, 12, 14-16, and 18-20 remain in the application. Claims 1, 12, 15, 16, 18, and 20 have been amended. Claims 10, 11, 13, and 17 have been canceled.

In the final Office Action mailed April 5, 2005, the Examiner rejected claims 1-8 as anticipated by Lur et al. (U.S. Patent No. 5,554,566, of record). Claims 1-6 and 9 were rejected under 35 U.S.C. § 102(e) as anticipated by Jenq et al. (U.S. Patent No. 5,893,751, of record). Claims 10-17 and 20 were rejected under 35 U.S.C. § 103(a) as obvious over Jenq et al. in view of U.S. Patent No. 5,937,325 ("Ishida"). Claims 18 and 19 were rejected as obvious over Jenq et al. in view of Ishida and further in view of Lur et al.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

In a telephone conference with the Examiner on May 27, 2005, applicant's undersigned representative discussed the teachings of the Ishida reference. More particularly, in the final Office Action mailed April 5, 2005, the Examiner states that Ishida "teaches a silicide film (68) on a polysilicon line (56), wherein the silicide is formed to enter a C-49 phase and not a C-54 phase (column 3, line 28 – column 4, line 39) for below 0.25 microns polysilicon dimensions to ensure a conversion to lower resistivity."

Applicant respectfully submits that while the portion of Ishida quoted by the Examiner does in fact teach entering a C-49 phase, it does so only for the source and drain regions 58, 60. Ishida does not teach that the gate region be formed to remain in the C-49 phase. Rather, Ishida teaches at column 4, lines 39-47 that the titanium silicide region 68 above only the polysilicon gate is subjected to a high temperature anneal to form the low resistivity C-54 titanium silicide phase 69, which is clearly shown in Figure 3e.

Turning to the claims, claim 1 is directed to an integrated semiconductor device that comprises a semiconductor material substrate, a polysilicon line forming a gate region, the polysilicon line having micro-rough indentations on a top surface of the polysilicon line formed by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line. Claim 1 further recites a silicide film covering the micro-rough top surface portion of the polysilicon line, the silicide film remaining in a C-49 phase and not later anodized to a C-54 phase.

Application No. 10/068,534
Reply to Office Action dated April 5, 2005

Now-canceled dependent claims 10 and 11 recited the silicide film formed to not enter a C-54 transformation phase but to enter a C-49 phase. Claims 10 and 11 were rejected as obvious over the combination of Jenq et al. and Ishida. However, in view of the teachings of Ishida that only the polysilicon gate is subjected to a high-temperature anneal to form a low resistivity C-54 titanium silicide phase, the combination of Jenq et al. and Ishida fails to teach or suggest the present invention. As applicant argued in the amendment submitted January 4, 2005, which arguments are incorporated in their entirety herein, Jenq et al. fails to teach or suggest a level of roughness recited in claim 1. The combination of Jenq et al. and Ishida falls short of claim 1 because the level of roughness recited therein and the silicide film remaining in a C-49 phase over the polysilicon line that forms a gate region is not taught by either reference, taken alone or in any combination thereof. Thus, applicant respectfully submits that claim 1 and dependent claims 2-9 are clearly allowable over the references cited by the Examiner.

Claim 12 is directed to an integrated circuit that includes a polysilicon line forming a gate region and formed to have micro-rough indentations on a top surface by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line. Claim 12 further recites a silicide formed on the micro-rough top surface of the polysilicon line, the silicide remaining in a C-49 phase and not later anodized to enter a C-54 transformation phase. Claim 12 was rejected over the combination of Jenq et al. and Ishida. Applicant respectfully submits that claim 12 is allowable for the reasons discussed above with respect to claim 1, *i.e.*, that the combination of Jenq et al. and Ishida fails to teach or suggest the recited combination of claim 12. Thus, claim 12 and dependent claim 14 are clearly allowable over the references.

Claim 15 is directed to a semiconductor device that includes, *inter alia*, a polysilicon line forming a gate region and a silicide film formed on a micro-rough top surface of the polysilicon line, the silicide film remaining in a C-49 phase. Applicant respectfully submits that claim 15 is allowable for the reasons discussed above with respect to claims 1 and 12, *i.e.*, that no combination of Jenq et al. and Ishida teach or suggest the recited combination of claim 15. Moreover, as discussed with the Examiner in a telephone conference on May 27, 2005, the recitation of the silicide film remaining in a C-49 phase is clearly distinguishable over the Ishida reference. Moreover, the recitation that the C-49 film is not later anodized to enter the C-54

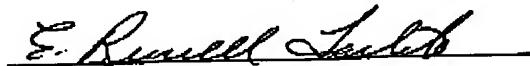
Application No. 10/068,534
Reply to Office Action dated April 5, 2005

phase is also distinguishable over the Ishida reference with respect to the polysilicon line forming a gate region.

Applicant respectfully submits that all of the claims remaining in this application are clearly in condition for allowance.

In the event the Examiner disagrees with the foregoing or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,
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